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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 21/331, 21/324, 21/265, 29/732, 29/417

A2

(11) International Publication Number: **WO 98/53489**

(43) International Publication Date: 26 November 1998 (26.11.98)

(21) International Application Number: PCT/SE98/00929

(22) International Filing Date: 18 May 1998 (18.05.98)

(30) Priority Data:
9701934-3 23 May 1997 (23.05.97) SE

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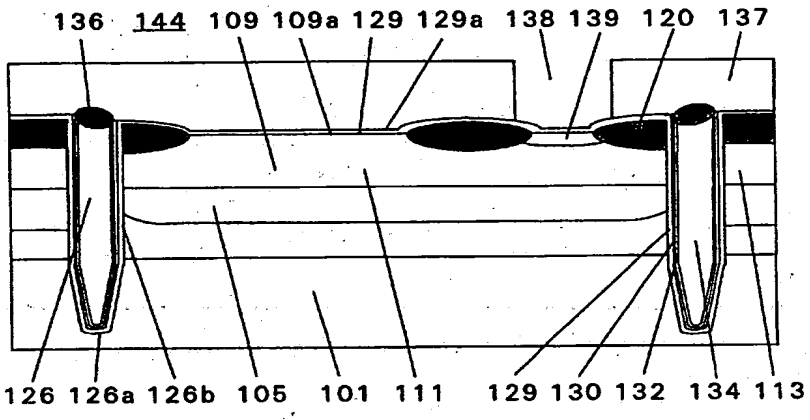
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: INTEGRATED CIRCUIT, COMPONENTS THEREOF AND MANUFACTURING METHOD



(57) Abstract

The present invention relates to a collector pin and a trench in an integrated circuit intended for high speed communication, and to a manufacturing method for these items. The collector pin is achieved by creating an area which is implantation damaged or made amorphous and at least partially doped (139) by means of ion implantation from an upper silicon surface comprised in a semiconductor structure (144) down to a depth lower than the depth of the surrounding field oxide (120), and that the semiconductor structure (144) is then heat treated. The trench (126) is achieved by uncovering a predetermined area of the upper silicon surface (109a), etching the semiconductor structure (144) within the predetermined area to a predetermined depth, uniformly depositing a first oxide layer (129), preferably of the type LPCVD-TEOS over the semiconductor structure, especially in the trench, uniformly depositing a barrier layer (130), preferably of silicon nitride, over the first oxide layer (129), filling the trench (126) by depositing a silicon layer (134, 135), which is subsequently etched back, over the nitride layer (130), especially in the trench (126), and thermally growing a cap oxide (136) over the trench filling (134).

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Integrated circuit, components thereof and manufacturing method

Technical Field

The present invention relates to a method for producing, in the manufacturing of an integrated circuit in a bipolar process, a collector pin and a trench for isolating the semiconductor components comprised in the integrated circuit, and to the collector pin, the trench and the integrated circuit. The collector pin, the trench and the integrated circuit are primarily intended for radio applications or other high-speed communication where components with good performance characteristics are required.

State of the Art

Traditionally, when manufacturing integrated circuits, so called LOCOS (Local Oxidation of Silicon) isolation is used in combination with junction isolation, to isolate the components of the integrated circuit; see, for example, J.A. Appels et al, "Local Oxidation of Silicon and its application in Semiconductor Technology,", Philips Res. Rep. vol. 25, 1970, pp. 118-132.

In the manufacturing of bipolar components for RF-IC (Radio Frequency - Integrated Circuits) applications, it is common to isolate the individual components in the silicon substrate from each other with etched trenches instead; see, for example, US 4,139,442, US 4,789,885, P.C. Hunt et al., "Process HE: A Highly Advanced Trench Isolated Bipolar Technology for Analogue and Digital Applications", Proc. IEEE 1988 Custom & Integr. Circuits Conf. Rochester N.Y. May 16-19 1988, and A. Hayasaka et al., "U-Groove Isolation Technique for High Speed Bipolar VLSI's", Proc. IEDM 1982 p. 62.

The technique of trench isolation has also been used for isolating CMOS components, although to a considerably smaller extent, see for example R.D. Rung et. al, "Deep trench isolated CMOS Devices", IEDM, Techn. Dig. Paper 9.6, 1982.

By means of a trench, etched deeply into the silicon, and surrounding a semiconductor component, such as, for example, a bipolar transistor, the capacitance between the bottom diffusion layer and the substrate can be reduced substantially. At the same time better isolation between adjacent components is achieved, that is, an increased immunity against cross talk, while the dimensions of the transistor cell may be reduced at the same time.

Another advantage of trench isolation is that the trenches may be made so deep, approx. 5-10 μm, that they extend through the entire epi-layer of the plate, that is, the active surface layer, all the way down to a heavily doped silicon substrate of low resistance. Thus, the isolating properties and the risk for latch-up are reduced, see for example V. dela Torre et al., "MOSAIC V-A Very High Performance Bipolar Technology", Proc. BCTM 1991, p. 21.

Below, and in connection with the figures 1-3, a commonly used method for making a trench when manufacturing a bipolar transistor of npn type is described.

As starting material a low doped p type monocrystalline silicone substrate 1 of (100) orientation, shown in Figure 1, is used. A heavily doped bottom diffusion layer of n type, or a buried collector layer 2, which may be made of, for example, an ion implanted layer of arsenic or antimony, is created, whereafter an epitaxic silicon layer 3 of n type is applied with a thickness of approximately 1-2 μm.

At least two variations as to where the so called trench module may be integrated in the process flow are known from the literature. According to a first variation,

described by, for example the mentioned P.C. Hunt et al. and US 4, 983, 226, the trench processing is performed before the definition (with LOCOS technique) of the field areas. According to the second variation, disclosed in, among other documents, EP 0, 724, 291 A2, the trench is created after the definition of the field areas. Both variations aim at the same final result, and in the following, only the first variation will be described.

A layer 4, approximately 1 μm thick, of LPCVD (Low Pressure Chemical Vapor Deposition) oxide, which will function as a hard mask, is then deposited over the plate. Trench openings 5a are then defined in a lithographic way, whereafter the oxide layer 4 is etched back to reveal the underlying silicon surface. Then all photo resist is removed from the structure, whereafter the epitaxial layer 3, the bottom diffusion layer 2 and the silicon substrate 1 are etched back using an anisotropic dry etching until a trench 5 of a predetermined depth, approximately 5-10 μm has been created (see Figure 1).

As the substrate is made up of lightly doped p type material, usually a small dose of low energy boron is implanted in the bottom of the trench 5 to achieve a channel stop 6, see Figure 2. The channel stop 6 reduces the current amplification of the parasite transistor (n+ bottom diffusion layer/p- substrate/n+ bottom diffusion layer) which is created and which increases the threshold voltage for the corresponding parasite MOS transistor. If, on the other hand, an epi-material of p-/p+ type is used as a starting material, no such implant is needed.

After the etching of the trench and the implantation of ions the hard mask 4 is removed, whereafter the semiconductor structure is oxidised thermally until a silicon oxide 7 approximately 100 nm is obtained. Then a thin silicon nitride layer 8 is deposited over the semiconductor structure, especially in the trench 5, whereafter the trench is filled with polysilicon 9. Alternatively an insulating or semi-insulating

substance, for example silicon oxide may be used, as described in US 4, 139,442 or the above mentioned R.D. Rung et al. The filling material, which in Hunt's article is made up of polysilicon, is etched back with dry etching until the silicon nitride layer 8 is uncovered outside the trench opening 5a.

After the filling substance 9 has been etched back, the silicon nitride layer 8 is masked and etched, whereafter silicon is oxidized by means of conventional LOCOS technique for creating both thick field oxide areas 10 and a cap oxide 11 over the trench opening, see Figure 3. If the trench 5 is already filled with oxide from the beginning, of course no additional cap oxidation is needed.

A collector pin 12, connecting the bottom diffusion layer 2 to the silicon surface, is obtained, whereafter remaining areas of the silicon nitride layer 8 and the silicon oxide layer 7 are removed. Figure 3 shows the structure resulting from this. As an alternative, the collector pin 12 can be implanted before the trench processing, as described in US 4,958,213.

The above described techniques have a number of drawbacks, which have led to a low yield being noticed when using trench isolation, see for example F. Yang et al. "Characterization of collector-emitter leakage in self-aligned double-poly bipolar junction transistors", J. Electrochem. Soc., vol. 140, no. 10, 1993, p. 3033.

The commonly accepted explanation of the low yield when trench isolation is used is that the trench process (trench etching, sidewall oxidation, filling, re-etching and cap oxidation) introduces defects in the silicon substrate. A relatively detailed description of the problems of trench isolation and suggestions on how to avoid them have been the subject of a number of patents, see for example US 4, 983, 226, EP 0, 278, 159 A2 and the above mentioned US 4, 958 213.

Also, the descriptions are not consistent, in the sense that in US 4, 958, 213 expresses the opinion that a thickness of the sidewall oxide in the trench of approximately 100 nm functions satisfactorily, whereas in US 4, 983, 226 an upper limit of 45 nm is recommended for the thickness of the oxide layer. Otherwise, according to US 4, 983, 226, unnecessary mechanical stress, and thereby dislocations, will be created.

In EP 0, 278 159 A2 it is described how a thin layer of polysilicon is deposited on the inside of the trench, which is later converted, in thermal oxidation, to oxide on the inside of the trench. In this way, unnecessarily heavy oxidation is avoided, and the mechanical tension or stress is reduced.

US 4, 958, 213 expresses the opinion that the cap oxidation step creates problems. Therefore it is suggested in a final step to refill the upper part of the trench opening with a deposited oxide to reduce the mechanical tension caused by the creation of so-called bird's beaks at cap oxidation. The suggestion both involves complicated process techniques and high manufacturing costs, since it requires two filling steps, which are independent, and following planarization.

In, for example, US 4, 983, 226, the use of cap oxide, which is simpler, is described. To eliminate the presence of vertical bird's beaks, it is suggested to use a thin layer of silicon nitride on top of the sidewall oxide in the trench and thereby minimize the mechanical stress. A similar method is described in the above mentioned P.C. Hunt et al.

In all the cases described above polysilicon or silicon oxide has been suggested as a filling material in the trenches. This may lead to the presence of voids in the filling, see for example Figure 7, page 577 in R.D. Rung's article.

Summary of the Invention

An object of the present invention is to provide an integrated circuit having at least one isolating trench, especially an integrated circuit intended for radio applications or other high speed communication, which is reliable and has good performance characteristics.

Another object of the invention is to provide a trench isolated integrated circuit avoiding one or more of the problems that can arise with prior art.

Yet another object of the invention is to provide an integrated circuit with trenches having no dislocations.

A further object of the invention is to provide a reliable and uncomplicated manufacturing method for an integrated circuit having the above-mentioned properties. In particular, a manufacturing method giving a high yield is strived for.

Other objects of the present invention will become apparent from the description below.

A problem which has not yet been given attention, is that even an integrated circuit with a trench completely without dislocations may be unreliable, unless a collector pin comprised in the integrated circuit can be made without dislocations. At ion implantation of the collector pin according to prior art, defects or dislocations are introduced, especially screw dislocations, which may be confined to the area enclosed by the trench. These defects can then penetrate active p-n junctions, whereby an increased leakage current arises. In the worst case, such an integrated circuit becomes useless.

By recognizing this problem, a reliable integrated circuit without dislocations may be manufactured by combining a trench without dislocations, according to prior art, with a manufacturing method for a collector pin without dislocations.

According to the invention, this method involves providing a collector opening by revealing a predetermined area surrounded by field oxide on an upper surface of silicon in a semiconductor structure by means of etching, providing an area that has been implantation damaged, or made amorphous, and at least partially doped extending from the upper silicon surface down to a depth lower than the depth of the field oxide, implanting ions of a predetermined dose and energy through the upper silicon surface and by subsequently heat treating the semiconductor structure.

Preferably the area is achieved in two steps, the first of which comprises making the surface region of the area amorphous, especially by implanting heavy ions, such as for example arsenic or antimony ions. The second step involves doping the area from its surface region down, especially by letting light ions, such as phosphorus ions be implanted.

The heat treatment is also preferably performed in two steps. First the area is recrystallized from the bottom up by heat treatment, preferably at approximately 550-600°C for approximately 1/2 - 1 hour. Then the doped ions, especially the phosphorus ions are caused to diffuse down towards a doped bottom diffusion layer comprised in the semiconductor structure by means of annealing, preferably at approximately 950°C for approximately 1 hour.

The invention also comprises an improved manufacturing method for the trench. An oxide layer, preferably of the kind PECVD (Plasma Enhanced Chemical Vapor Deposition) TEOS, is uniformly deposited over the semiconductor structure,

especially in the trench. Before the filling of the trench a barrier layer of silicon nitride is deposited as well.

In more detail, the method according to the invention involves the deposition of a hard mask, especially an oxide layer of the kind PECVD (Plasma Enhanced Chemical Vapor Deposition) the deposition of TEOS over a semiconductor structure comprising an upper silicon surface, the creation of a trench opening by, through etching, uncovering of a predetermined area of the upper silicon surface, the creation of a trench by etching of the semiconductor structure within the predetermined area to a predetermined depth, the removal of the hard mask and the first silicon layer by means of etching, the uniform deposition of a first oxide layer, preferably of the kind LPCDV-TEOS, over the semiconductor structure, especially in the trench, the deposition of a barrier layer, preferably of silicon nitride uniformly over the first oxide layer, the depositing of a silicon layer over the silicon nitride layer, especially in the trench, to fill the trench, and the etching of the silicon layer until the underlying nitride layer is uncovered outside of the trench opening, and the thermal growing of a cap oxide over the trench opening.

Preferably the upper silicon surface is covered by an oxide before a first silicon layer, preferably of polysilicon, is deposited over the oxide before the hard mask is deposited.

The method according the invention may also comprise the creation of a tapered trench with a rounded bottom, wet etching and growing a thin thermal oxide before the first oxide layer is deposited, densifying the first oxide layer, depositing a second oxide layer on the nitride layer and filling the trench with microcrystalline silicon. Further improvement of the details will become apparent from the description below.

By means of the present invention, a reliable integrated circuit, with a trench that meets the requirements well, is obtained.

An advantage of the invention is that a relatively simple trench, substantially dislocation-free, may be used in combination with the collector pin according to the invention.

Another advantage is that when an oxide is deposited in the trench less tension is caused than if the oxide is grown thermally. Thus, the oxide may be deposited as a thicker layer, for example approximately 100-200 nm thick, which gives better isolation. If the oxide is densified, the isolating properties will be further improved.

Yet another advantage of the invention is that if the trench is given a tapered shape with a rounded bottom, the risk of mechanical tension and the creation of voids at the filling is reduced. This risk is further reduced if microcrystalline silicon is used for the filling.

Brief Description of the Drawings

The invention will be described in more detail in the following, with reference to the accompanying drawings, that is Figures 4-8, which are only shown to illustrate the invention and therefore should not in any way limit it.

Figures 1-3 illustrate, as cross sectional views, a method for manufacturing a trench and a collector pin during the manufacturing of an integrated circuit, according to prior art.

Figures 4-7 illustrate, as cross sectional views, a method for manufacturing a trench during the manufacturing of an integrated circuit, according to the present invention.

Figure 8 illustrates, as a cross-sectional view, a method for manufacturing a collector pin when manufacturing an integrated circuit according to the present invention.

Preferred Embodiments

Figure 4 shows a cross section of a silicon structure 100 of so called epi type which is characterized in that on a heavily doped substrate 101 (approximately 10 mΩ*cm) of p type, a lightly doped epi layer 103 (approximately 20 Ω*cm), also of p type, has been grown. The grown epi layer 103 is typically 5-10μm thick.

By starting from a so called epi material of p-/p+ type, no channel stop implant is needed (see the description of the state of the art), which in itself may introduce silicon damages. Boron does not fit the lattice structure of the silicon well, that is, the lattice match is poor.

A protective layer of silicone oxide is deposited on the structure in a way common in the art, for example by thermal oxidation. The oxide layer is masked lithographically before the oxide is removed in the areas which are not protected by resist. A bottom diffusion layer 105, a so called buried collector layer, of n+ type is then introduced in the silicon, by means of ion implantation. A subsequent heat treatment then drives the dopant of n type in to the desired depth, whereafter all the oxide is removed and the structure is globally implanted with a light dose of boron, so that a p doped area 107 is formed. Through this process a height difference or step 106 is achieved between the upper surface 105a of the bottom diffusion layer and the surface of the remaining structure. An approximately 1μm thick epitaxic layer 109 is then grown over the structure so that the surface 109a of this layer also comprises a step 108.

Then the epitaxic surface layer 109 will be doped selectively, according to a well known so called twin well method, to obtain areas of n and p type respectively, so called n well 111 and p well 113, see Figure 5. This may be done in a way similar to the one described in US 4, 958, 213 or in L.P. Parillo et al., "Twin-tub CMOS - A technology for VLSI circuits", IEDM Tech. Dig. 1980, p. 752. In this way, the step 108 in the surface 109a is strengthened.

In the n area 111, which is located directly on top of the bottom diffusion layer 105, active semiconductor components will be placed. Field oxide areas 120 are then defined over the structure, with well known LOCOS technique, whereafter a Kooi oxide 121 is thermally grown over the structure. This Kooi oxide 121 is typically 30-40 nm thick. The structure 118 obtained after the processing described above, before the trench module is started, is shown in Figure 5. Note that there is a step 115 in the surface 120a of the field oxide above the junction between the n well 111 and the p well 113.

The trench module is started, after Kooi oxidation, by depositing a thin layer 122, typically approximately 50 nm thick and of polysilicon, preferably by means of LPCVD technique over the structure, see Figure 6. On top of said polysilicon layer 122 a hard mask is deposited, which is preferably comprised of an approximately 300 nm thick oxide layer 124. Preferably the oxide is PECVD-TEOS.

A trench opening 125 is then defined lithographically, whereafter the oxide layer 124, the polysilicon layer 122 and the field oxide 120 are etched back with dry etching so that the underlying silicon surface is uncovered. This can suitably be done sequentially in a plasma etching system of multi chamber type. Conventional $CHF_3/CF_4/Ar$ chemistry is used for the oxide etching and Cl_2/HBr chemistry for the polysilicon etching. In the uncovered opening 125, a trench 126 will be created.

The photo resist is removed, whereupon the areas 111, 113, the bottom diffusion layer 105, the layer 103 and the substrate 101 are etched back with anisotropic dry etching, preferably with $NF_3/HBr/He/O_2$ chemistry, until the trenches 126 have obtained the desired depth, preferably approximately 5-10 μm. A dry etching process of several steps is used with advantage according to the invention to give the trench a tapered shape, especially the last micrometers, and a rounded bottom 126a, see Figure 6. The tapered shape facilitates the subsequent filling of the trench and the rounded trench bottom 126a reduces the effects of mechanical tension.

When the trench etching is finished, the oxide layer 124 and the underlying polysilicon layer 122, which has served as an etch stop at the removal of the oxide layer 124, are removed. The resulting structure 127 is shown in Figure 6.

Note that no channel stop implant of boron down in the trench 126 is needed in this case, as the trench 126 extends down in the p+ substrate 101. Thus, there is no risk of inversion along the trench bottom 126a. Said boron implant should be avoided, since it can cause dislocations in the silicon.

After the trench etching, according to the invention, a small amount of silicon (approximately 20 nm) is removed from the bottom 126a and sidewalls 126b of the trench by means of wet etching/cleaning, preferably in SC-1, that is, $NH_4OH/H_2O_2/H_2O$, which has been heated to approximately 80°C in a well known manner, see for example W. Kern et al. "Cleaning solution based on hydrogen peroxide for use in semiconductor technology", RCA Rev. June 1970, p. 187. In this way any pollution, such as metals and surface damages in the silicon caused in the trench etching are removed, which could later have caused dislocations in the silicon and thus low yield. Then the Kooi oxide 121 is removed with wet etching.

From several of the previously referenced patents it is evident that oxidation of the trench walls 126b may cause the formation of dislocations for example by the introduction of mechanical tension. To eliminate this risk, according to the invention a thin uniform oxide layer 129 is deposited, preferably TEOS, of a thickness of 50-200 nm by means of LPCVD technique over the structure, see Figure 7. As the LPCVD-TEOS layer 129 has a good step coverage, the layer 129 along the sidewalls 126a and the bottom 126a of the trench is achieved. Alternatively another type of oxide is deposited, using another deposition technique, for example PECVD or SACVD (Sub-Atmospheric Chemical Vapor Deposition) technique. The important thing is that an even, uniformly deposited oxide is provided in the trench 126.

Said oxide layer 129 should then be densified, especially at approximately 900 °C in an oxygen environment. Hereby the isolating properties of the oxide layer are improved. Also, one is not restricted to a maximum oxide thickness of approximately 45 nm which is described in the state of the art. Instead the TEOS layer may be deposited to a substantially higher thickness of the order of magnitude of 100-200 nm, without the mechanical tension increasing too much. In this way, the isolating properties of the trench 126 are substantially improved. Alternatively a thinner, not thicker than 50 nm, but preferably 10 nm thick thermal oxide may be grown along the sidewalls 126b and the bottom 126a of the trench before the LPCVD-TEOS layer is deposited (not shown in the figures).

After densifying the TEOS layer 129 a thin, approximately 50 nm thick barrier layer 130 of preferably silicon nitride is deposited over the structure and down in the trench 126. On top of the barrier layer 130, preferably a thin, approximately 30 nm thick TEOS layer 132 is deposited with LPCVD technique. This TEOS layer 132 later serves as an etch stop when etching back the trench filling.

In the trench 126, thus a laminate consisting of densified TEOS/silicon nitride/TEOS 129, 130 132 will be present - or alternatively a four layer laminate of thermal oxide/densified TEOS/silicon nitride/TEOS 129, 130, 132.

The trench 126 is then filled by depositing an approximately 1μm thick silicon layer 134, 135 over the structure using LPCVD technique, whereby the trench 126 is completely filled with the silicon. Preferably according to the invention microcrystalline silicone is used instead of polysilicon, since the risk of incomplete filling, that is, the creation of voids, is reduced.

After the filling, excess microsilicon 135 is removed from the surface by means of plasma etching. The etching is stopped when the TEOS layer 132 has been uncovered outside the trench opening 125. The obtained structure 132 is shown in Figure 7. Note that the upper surface 134a of the silicon filling comprises a step and thus is at least partially tilted.

Subsequently an approximately 300 nm thick cap oxide 136 is grown thermally over the trench opening 125, see Figure 8. This preferably takes place in a humid atmosphere at approximately 950°C. After the cap oxidation is ended the TEOS layer 132 and the underlying nitride layer 130 are removed, for example by means of dry etching. In this case, the surface of the TEOS layer functions as an etch stop.

The structure can then be masked with a photo resist 137 and if necessary etched to achieve the definition of a collector opening 138, which is to be surrounded by field oxide 120 The etching may be stopped on the upper silicon surface 109a, but the TEOS oxide 129 may also be left in the collector opening 138.

An implantation damaged or amorphous and at least partially doped area 139 is then achieved from the upper silicon surface 109a down to a depth lower than the depth

of the field oxide 120. This happens by ions of a predetermined dose or doses and energies being implanted through the upper silicon surface 109a. The obtained structure 144 which is shown in Figure 8, is heat treated after removal of the photo resist 137, in part for the area 139 to heal/recrystallize and in part for the dopants to diffuse down towards the bottom diffusion layer 105 and create electric contact with it.

Normally, the field oxide 120 is grown to a thickness of at least 500 nm. To observe the desired safety margins the damaged area 139 is thus achieved to a maximum depth of approximately 200 nm.

To avoid problems with formation of dislocations or defects at the heat treatment, that is, the recrystallization, the implantation is preferably carried out in two steps.

In a first step the surface region of the area, comprising the silicon surface 109a and an upper region of the area 139, is made amorphous, especially through the implantation of heavy ions, such as, for example, arsenic, antimony or argon ions. Preferably arsenic ions are used at a dose of the order of magnitude of $1*10^{15}$ ions/cm^2 and with an energy of the order of magnitude of 80 keV.

In the second step the area 139 is doped from its surface region down, especially by the implantation of light ions such as phosphorus ions. Suitable parameters here are a dose of the order of magnitude of $3*10^{15}$ ions/cm^2 and an energy of the order of magnitude of 50 keV. The parameters are adapted so that the main part of the implantation damages are kept within the surface region which has already been made amorphous.

The heat treatment is also preferably carried out in two steps, a recrystallization step and a diffusion step.

The area 139 is recrystallized from the bottom up by heat treatment, preferably at approximately 550-600°C for approximately 1/2-1 hour. In the recrystallization the damaged area will be healed from the bottom up while keeping the original crystal orientation. Hereby the arising of crystal defects, twins or screw dislocations is avoided. The latter, screw dislocations, are especially troublesome at trench isolation as they tend to be locked up in the area surrounded by the trench. These defects may then penetrate the active p-n junctions of the bipolar transistor, thus causing increased leakage currents.

If the implantation energy is selected too high, the surface layer will not be made amorphous, but instead an amorphous (damaged) region will be obtained between the surface layer and the inner part of the crystal. At subsequent heat treatment, these areas (the surface layer and the inner part of the crystal) will both serve as a substrate for regrowth of the grid. When the fronts meet, crystal defects arise. From, for example US 4, 958, 213, it is clear that both the implantation energy and the dose of phosphorus have been selected so that the latter case will arise, with resulting dislocation problems.

Finally, the doped ions, especially the phosphorus ions, are made to diffuse down towards the doped bottom diffusion layer or the buried collector layer 105 through annealing, preferably at approximately 950°C for about 1 hour. Hereby an electric connection to said bottom diffusion layer 105 is created.

The continued processing, that is, the making of active components, metallizing, etc., is done in ways well known in the art and will not be described in more detail here.

An integrated circuit manufactured according to the preferred method described above, according to the invention, is reliable and has good performance characteristics.

By achieving a collector pin without dislocations a previously ignored problem of, in some cases, low yield, has been solved. The collector pin can be combined with a trench, substantially without dislocations according to well known techniques, but is preferably used together with the trench according to the invention.

The disclosed trench may be made more effective than before by depositing an oxide, preferably an LPCVD-TEOS oxide and a barrier layer, especially of silicon nitride, in the trench before the filling.

Hereby an oxide thickness up to at least 200 nm is allowed without introducing an extent of tensions and/or defects, such as dislocations, which may damage the integrated circuit. A further oxide layer may be deposited on the barrier layer.

The integrated circuit with the collector pin according to the invention and/or the inventive trench are particularly well suited for radio and other high frequency applications.

Of course, the invention is not limited to the embodiments described above and shown in the drawings, but may be modified within the scope of the appended patent claims. The invention is obviously not limited as regards choice of material, dimensions, such as layer thicknesses or geometries.

In addition, the invention also comprises the creation of the trench earlier in the process, especially before the growing of the field oxide areas, creating the collector

pin before the creation of the trench as well as the creation of the inventive collector pin in combination with a trench made in any conventional manner.

Claims

1. A method for manufacturing a collector pin in a bipolar process in the manufacturing of an integrated circuit, especially an integrated circuit intended for radio applications or other high speed communication, said integrated circuit comprising a substantially dislocation-free isolating trench,
characterized by
- achieving a collector opening (138) by uncovering, by means of etching, a predetermined area, surrounded by field oxide (120), of an upper silicon surface (109a) or oxide surface (129a) comprised in a semiconductor structure (144),
- creating an area which is implantation damaged, or made amorphous, and at least partially doped (139) from the upper silicon surface down to a depth lesser than the depth of the field oxide by implantation of ions of a predetermined dose and energy through the upper silicon surface (109a), and
- subsequently heat treating of the semiconductor structure (144).

2. A method according to claim 1, **characterized** in that the surface region of the area is made amorphous, especially by the implantation of heavy ions, such as for example arsenic of antimony ions.

3. A method according to claim 2, **characterized** by the implantation of arsenic ions of a dose of the order of magnitude of $1*10^{15}$ ions/cm^2 and having an energy of the order of magnitude of 80 keV.

4. A method according to claim 2 or 3, **characterized** by doping the area (139) from its surface region down, especially by the implantation of light ions such as phosphorus.

5. A method according to claim 4, **characterized** by implanting phosphorus ions of a dose of an order of magnitude of $3*10^{15}$ ions/cm^2 and having an energy of an order of magnitude of 50 keV.

6. A method according to any one of the claims 1-5, **characterized** in that the area (139) is achieved to a maximal depth of approximately 200 nm and that the thickness of the surrounding field oxide (120) is selected to be at least 500 nm.

7. A method according to any one of the claims 1-6, **characterized** in that the area (139) is recrystallized from the bottom up by means of heat treatment, preferably at approximately 550-600°C for approximately 1/2-1 hour.

8. A method according to any one of the claims 1-7, **characterized** in that the doped ions are caused to diffuse down towards a bottom diffusion area (105) comprised in the semiconductor structure (144), through annealing, preferably at approximately 950°C for about 1 hour.

9. A method for use in the manufacturing of an integrated circuit, especially of an integrated circuit intended for radio applications or other high speed communication, for achieving an isolation of the semiconductor components comprised in the integrated circuit,
characterized by
- depositing a hard mask (124), especially an oxide layer, of the kind PECVD-TEOS, over a semiconductor structure (118), comprising an upper silicon surface (109a),
- achieving a trench opening (125) by uncovering, by means of etching, a predetermined area of the upper silicon surface (109a),
-achieving a trench (126) by etching the semiconductor structure thus obtained within the predetermined area to a predetermined depth,
-removing the hard mask (124) and the first silicon layer (122) by means of etching,

- uniformly depositing a first oxide layer (129), preferably of the kind LPCVD-TEOS, over the semiconductor structure (127), especially in the trench (126),
- uniformly depositing a barrier layer (130), preferably of silicon nitride, over the first oxide layer (129),
- filling the trench (125) by depositing a silicon layer (134, 135) over the barrier layer (130), especially in the trench (125) and etching back the silicon layer (134, 135), and
- thermally growing a cap oxide (136) over the trench opening (134).

10. A method according to claim 9, **characterized** in that the upper silicon surface (109a) is covered by an oxide (121, 120) and that a first silicon layer (122), preferably of polysilicon, is deposited over the oxide (121, 120) before the hard mask (124) is deposited.

11. A method according to claim 9 or 10, **characterized** in that the oxide cover (121, 120) is selected to be comprised, at least in part, of field oxide (120).

12. A method according to any one of the claims 9-11, **characterized** in that the trench (126) is cleaned by means of wet etching before the first oxide layer (129) is deposited.

13. A method according to claim 12, **characterized** in that the wet etching is performed with heated SC-1.

14. A method according to any one of the claims 9-13, **characterized** in that a thin thermal oxide is grown in the trench before the first oxide layer (129) is deposited.

15. A method according to any one of the claims 9-14, **characterized** in that the trench (126) is given a tapered shape and preferably a depth of approximately 5-8 µm.

16. A method according to any one of the claims 9-15, **characterized** in that the bottom (126a) of the trench is made to be rounded.

17. A method according to any one of the claims 9-16, **characterized** in that the first oxide layer (129) is densified, preferably in an oxygen environment at approximately 900°C.

18. A method according to any one of the claims 9-17, **characterized** in that the first oxide layer (129) is deposited to a thickness of approximately 50-200 nm.

19. A method according to any one of the claims 9-18, **characterized** in that a second oxide layer (132), preferably of the kind LPCVD-TEOS, is deposited uniformly over the barrier layer (130), especially in the trench (126), before the trench (126) is filled, and that said second oxide layer (132) is used as an etch stop when the silicon layer (134, 135) is etched back.

20. A method according to any one of the claims 9-19, **characterized** in that the silicon layer (134, 135) is made up of microcrystalline silicon.

21. A method according to any one of the claims 9-20, **characterized** in that the cap oxide (136) is grown to an individually selected thickness.

22. A method according to any one of the claims 11-21, **characterized** in that a doped bottom diffusion area (105) is achieved in such a way that a step (108) is created in the silicon surface (109a) before covering with oxide.

23. A method according to claim 22, **characterized** in that an n well (111) and a p well (113) are obtained by the doping of an epitaxic layer (109) comprised in the semiconductor structure (110) in a twin well procedure, wherein the step (108), which is further strengthened, is selected to be located between the n well (111) and the p well (113).

24. A method according to claim 23, **characterized** in that the field oxide (120) is achieved, especially according to LOCOS technique, over the border area between the n well (111) and the p well (113), before the deposition of the first silicon layer (122), whereby a step (115) is obtained in the field oxide surface (120a).

25. A method according to claim 24, **characterized** in that the predetermined area of the upper silicon surface (109a) of the semiconductor structure, which is uncovered to achieve the trench opening (125), is selected to comprise the step (108) obtained between the n well (111) and the p well (113).

26. A method according to any one of the claims 9-25, **characterized** in that the oxide cover is selected to be comprised, at least in part, of a Kooi oxide (121) and that said Kooi oxide (121) is removed, preferably before the deposition of the first oxide layer (129).

27. A method according to any one of the claims 9-26, **characterized** in that a dislocation-free collector pin is produced by

- achieving a collector opening (138) by uncovering, by means of etching, a predetermined area of the upper silicon surface (109a) or the oxide surface (129a), surrounded by field oxide (120),
-achieving an area (139) which is implantation damaged or made amorphous and at least partially doped from the upper silicon surface (109a) down to a depth lower

than the depth of the field oxide, by the implantation of ions of a predetermined dose and energy through the upper silicon surface (109a), and
-heat treating the semiconductor structure obtained in this way.

28. A method according to claim 27, **characterized** in that the surface region of the area is made amorphous, especially by the implantation of heavy ions such as for example, arsenic or antimony ions.

29. A method according to claim 27 or 28, **characterized** in that the area (139) is doped from its surface region down, especially by the implantation of light ions, such as phosphorus ions.

30. A method according to any one of the claims 27-29, **characterized** in that the area (139) is recrystallized from the bottom up by heat treatment and that the doped ions are made to diffuse down towards a doped bottom diffusion area (105) comprised in the semiconductor structure (144) by means of annealing.

31. A collector pin in a bipolar integrated circuit with an isolating, substantially dislocation-free trench, especially in a bipolar integrated circuit intended for radio applications or other high speed communication, **characterized** by
- a collector opening (138) obtained by uncovering a predetermined area of an upper silicon surface (109a) or oxide surface (129a) comprised in a semiconductor structure (144) and surrounded by field oxide (120),
-an area (139), without dislocations and at least partially doped, from the area of the upper silicone surface surrounded by field oxide (120) down towards a doped bottom diffusion area (105) comprised in the semiconductor structure (144), achieved through a substantially superficial ion implantation, followed by a recrystallization from the bottom up, and diffusion.

32. A collector pin according to claim 31, **characterized** in that the surface region of the area comprises implanted arsenic or antimony ions and that the regions of the area below the surface region comprise implanted and diffused phosphorus ions.

33. Bipolar transistor in an integrated circuit with an isolating trench, substantially dislocation-free, especially in an integrated circuit intended for radio applications or another high speed communication, **characterized** by
- a collector opening (138) achieved by the uncovering of a predetermined area of an upper silicon surface (109a) or oxide area (129a) comprised in a semiconductor structure (144) and surrounded by field oxide (120),
a dislocation-free and at least partially doped area (139) from the area on the upper silicon surface surrounded by field oxide (120) down towards a doped bottom diffusion area (105) comprised in the semiconductor structure (105) and achieved through a substantially superficial ion implantation, followed by recrystallization from the bottom up, and diffusion.

34. A trench for isolating semiconductor components comprised in an integrated circuit, said integrated circuit being especially intended for radio applications or other high speed communication, **characterized** by
- an etched trench (126) having a predetermined shape and depth within a predetermined area in a semiconductor structure (144),
- a first oxide layer (129), preferably of the type LPCVD-TEOS, uniformly deposited in the trench (126),
- a barrier layer (130), preferably of silicon nitride, uniformly deposited over the first oxide layer (129),
- a silicon filling (134) and
- a cap oxide (136) thermally grown over the silicon filling (134).

35. A trench according to claim 34, **characterized** by a tapered width and a rounded bottom (126a).

36. A trench according to claim 34 or 35, **characterized** by a depth of approximately 5-8 μm.

37. A trench according to any one of the claims 34-36, **characterized** in that the first oxide layer (129) is densified and approximately 50-200 nm thick.

38. A trench according to any one of the claims 34-37, **characterized** by a second oxide layer (132), preferably of the type LPCVD-TEOS, uniformly deposited over the barrier layer (130) in the trench (126).

39. A trench according to any one of the claims 34-38, **characterized** in that the silicon filling (134) is made up of microcrystalline silicon.

40. A trench according to any one of the claims 34-39, **characterized** by a field oxide area (120), surrounding the upper parts of the trench.

41. A trench according to any one of the claims 34-40, **characterized** in that the upper surface of the silicon filing (134a) comprises a step.

42. An integrated circuit with isolating, substantially dislocation-free trenches, especially an integrated circuit intended for radio applications or other high speed communication, **characterized** by a collector pin, comprising
- a collector opening (138) achieved by the uncovering of a predetermined area of an upper silicon surface (109a) or oxide surface (129a), comprised in a semiconductor structure (144) and surrounded by field oxide (120),

- a dislocation-free and at least partially doped area (139) from the area in the upper silicon surface surrounded by field oxide (120) down towards a doped bottom diffusion area (105) comprised in the semiconductor structure (144), achieved through a substantially superficial ion implantation, followed by recrystallization from the bottom up, and diffusion.

43. An integrated circuit, especially an integrated circuit intended for radio applications or other high speed communication, **characterized** by a trench, comprising
- an etched trench (126) of predetermined shape and depth, etched within a predetermined area in a semiconductor structure (144),
- a first oxide layer (129), preferably of the type LPCVD-TEOS, uniformly deposited in the trench (126),
- a barrier layer (130), preferably of silicon nitride, uniformly deposited over the first oxide layer (129),
a silicon filling (134), and
- a cap oxide (136), thermally grown over the silicon filling (134).

44. An integrated circuit according to claim 43, **characterized** by a collector pin, comprising
- a collector opening (138), achieved by the uncovering of a predetermined area of an upper silicon surface (109a) or oxide surface (129a) comprised in a semiconductor structure (144) and surrounded by field oxide (120),
- a dislocation-free and at least partially doped area (139) from the area in the upper silicon surface surrounded by field oxide (120) down towards a doped bottom diffusion area (105) comprised in the semiconductor structure (144) and achieved in a substantially superficial ion implantation, followed by recrystallization from the bottom up, and diffusion.

Prior Art

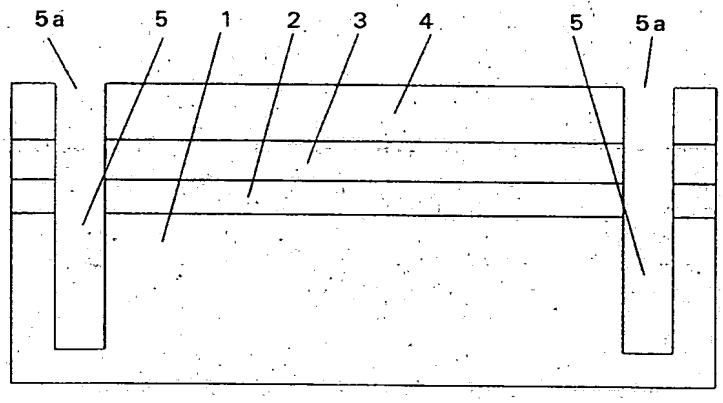


Fig. 1

Prior Art

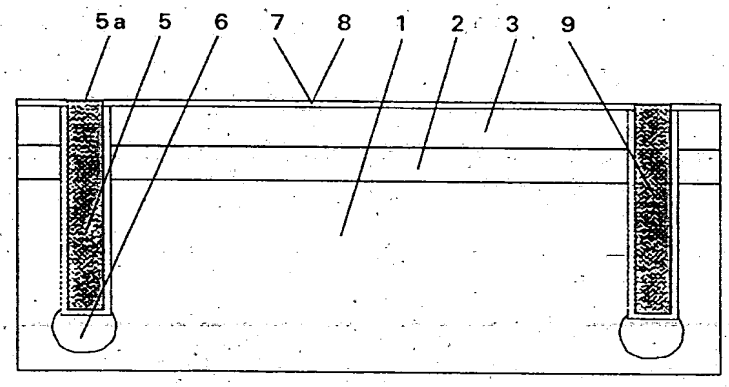


Fig. 2

Prior Art

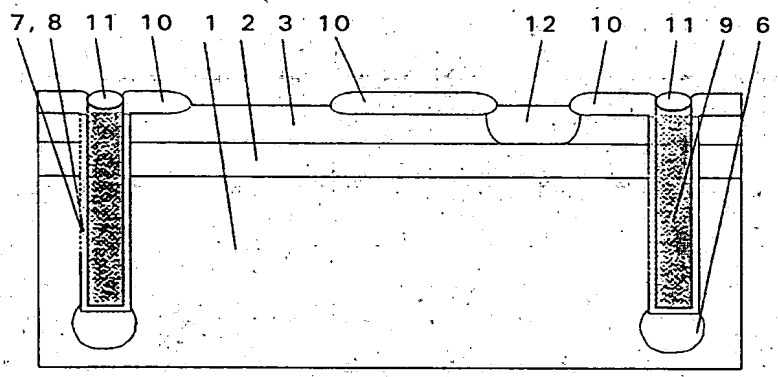
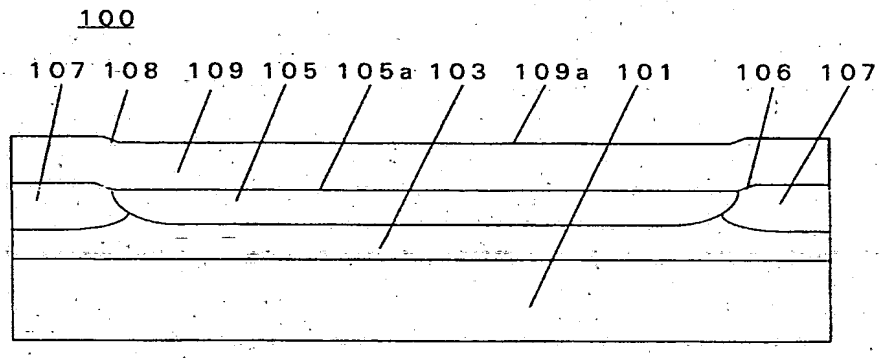


Fig. 3



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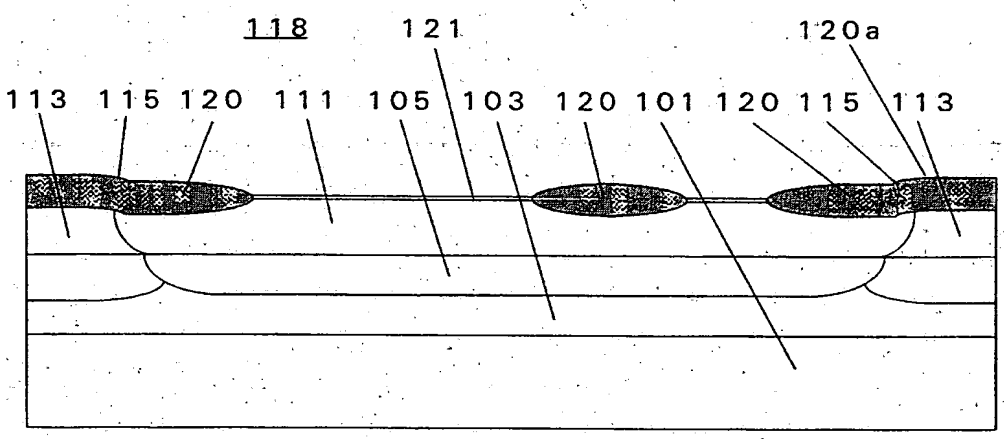
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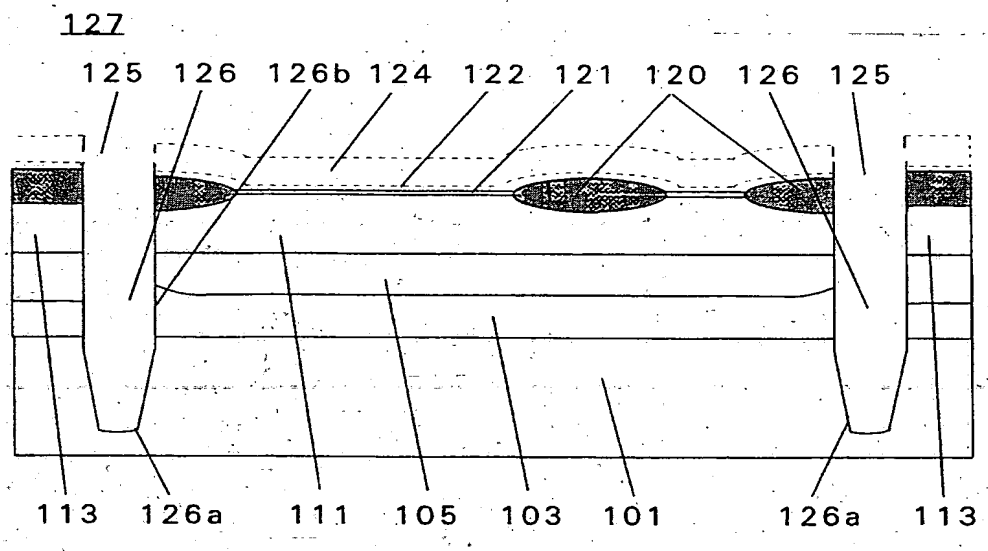
113

Fig. 5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126
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113
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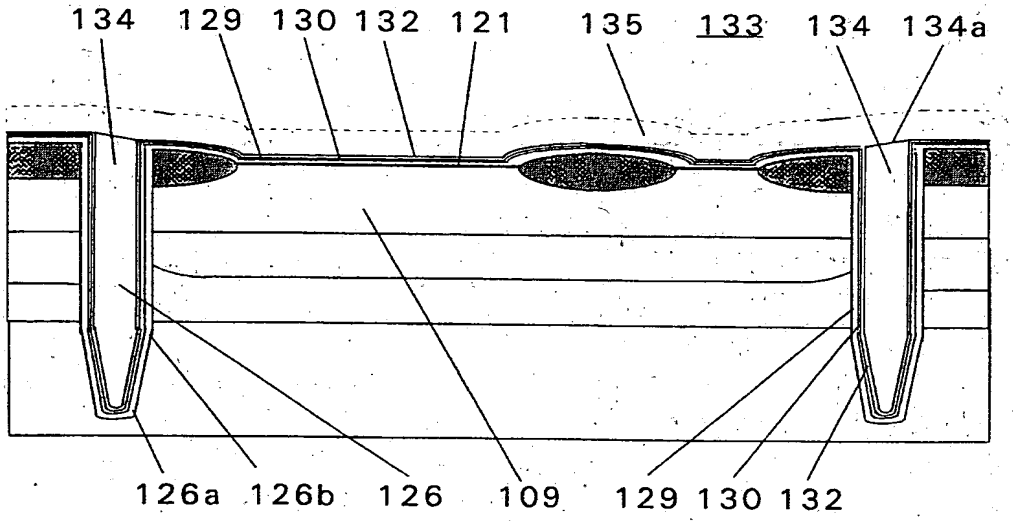
126a
113

Fig. 6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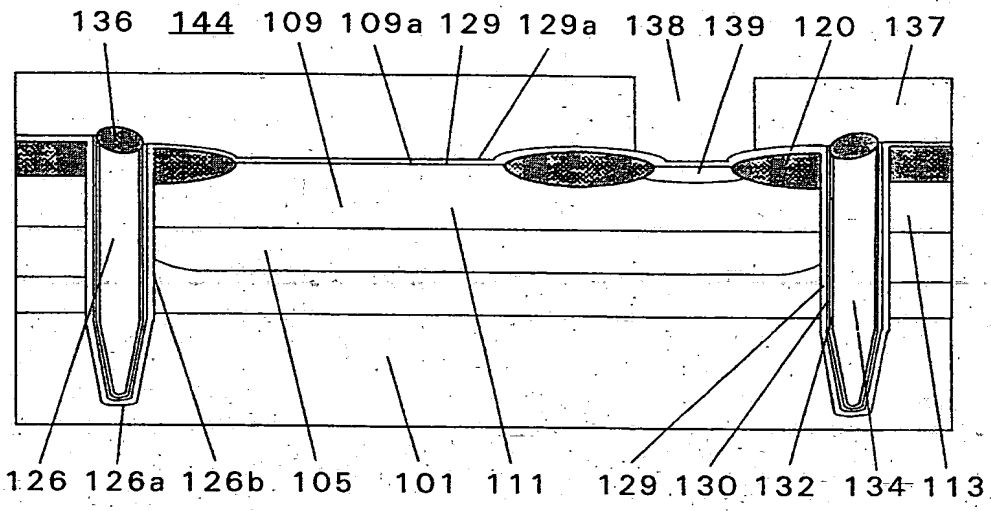
132

Fig. 7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132
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113

Fig. 8

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/331, 21/324, 21/265, 29/732, 29/417 — A3

(11) International Publication Number: **WO 98/53489**

(43) International Publication Date: 26 November 1998 (26.11.98)

(21) International Application Number: PCT/SE98/00929

(22) International Filing Date: 18 May 1998 (18.05.98)

(30) Priority Data:
9701934-3 23 May 1997 (23.05.97) SE

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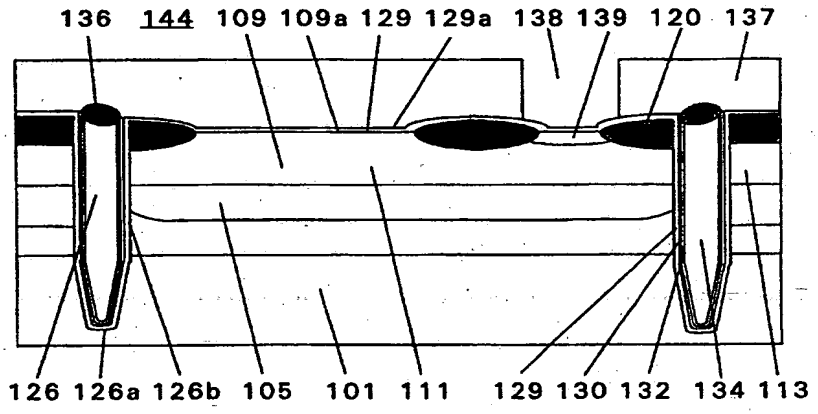
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(88) Date of publication of the international search report:
11 March 1999 (11.03.99)

(54) Title: INTEGRATED CIRCUIT, COMPONENTS THEREOF AND MANUFACTURING METHOD



(57) Abstract

The present invention relates to a collector pin and a trench in an integrated circuit intended for high speed communication, and to a manufacturing method for these items. The collector pin is achieved by creating an area which is implantation damaged or made amorphous and at least partially doped (139) by means of ion implantation from an upper silicon surface comprised in a semiconductor structure (144) down to a depth lower than the depth of the surrounding field oxide (120), and that the semiconductor structure (144) is then heat treated. The trench (126) is achieved by uncovering a predetermined area of the upper silicon surface (109a), etching the semiconductor structure (144) within the predetermined area to a predetermined depth, uniformly depositing a first oxide layer (129), preferably of the type LPCVD-TEOS over the semiconductor structure, especially in the trench, uniformly depositing a barrier layer (130), preferably of silicon nitride, over the first oxide layer (129), filling the trench (126) by depositing a silicon layer (134, 135), which is subsequently etched back, over the nitride layer (130), especially in the trench (126), and thermally growing a cap oxide (136) over the trench filling (134).

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INTERNATIONAL SEARCH REPORT

Inte...ational application No.
PCT/SE 98/00929

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 21/331, H01L 21/324, H01L 21/265, H01L 29/732, H01L 29/417
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOG: WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0724291 A2 (NEC CORPORATION), 31 July 1996 (31.07.96), page 17, line 29 - page 19, line 48, figures 7-8E,11,16	1-3,6-8, 31-33,42
A	--	4,5
Y	US 4980747 A (LOUIS N. HUTTER ET AL), 25 December 1990 (25.12.90), see the whole document	1-3,6-8, 31-33,42
A	--	4,5,9-30, 34-41,43,44

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Date of the actual completion of the international search	Date of mailing of the international search report
2 December 1998	03 -12- 1998
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International application No.
PCT/SE 98/00929

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4301588 A (CHENG T. HORNG ET AL), 24 November 1981 (24.11.81), see the whole document	1-3,6-8, 31-33,42
A		4,5
	--	
A	US 4789885 A (JEFFREY E. BRIGHTON ET AL), 6 December 1988 (06.12.88), see the whole document	1-8,31-33,42
	--	
A	US 5266504 A (JEFFREY L. BLOUSE ET AL), 30 November 1993 (30.11.93), see the whole document	1-8,31-33,42
	--	
A	PROCEEDINGS OF THE 1991 BIPOLAR CIRCUITS AND TECHNOLOGY...., Volume, September 1991, (MINNEAPOLIS), V. Dela Torre et al, "MOSAIC V - A Very High Performance Technology", page 21 - page 24, figure 1A	1-8,31-33,42
	--	
A	Proceedings of the IEEE 1988 CUSTOM INTEGRATED CIRCUITS...., Volume, May 1988, (NEW YORK), P.C. HUNT ET AL, "PROCESS HE: A HIGHLYADVANCED TRENCH ISOLATED BIPOLAR TECHNOLOGY FOR ANALOQUE AND DIGITAL APPLICATIONS", figure 1C, see page 22.2.1 - 22.2.4	1-8,31-33,42
	--	
A	US 5592412 A (RICHARD KLEINHENZ ET AL), 7 January 1997 (07.01.97), column 3, line 1 - line 28, figures 1-2	9-30,34-41, 43,44
	--	
A	WO 9525343 A1 (NATIONAL SEMICONDUCTOR CORPORATION), 21 Sept 1995 (21.09.95), page 2, line 40 - page 4, line 19, figures 1-9	9-30,34-41, 43,44
	--	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 98/00929

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5217920 A (ROBERT J. MATTOX ET AL), 8 June 1993 (08.06.93), column 2, line 19 - column 4, line 67, figures 1-6 --	9-30,34-41, 43,44
A	US 5270265 A (DONALD F. HEMMENWAY ET AL), 14 December 1993 (14.12.93), column 3, line 9 - column 4, line 63, figures 4-9, abstract --	1-44
A	US 4958213 A (ROBERT H. EKLUND ET AL), 18 Sept 1990 (18.09.90), column 6, line 23 - column 7, line 39, figures 7a-c, abstract --	9-30,34-41, 43,44

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 98/00929

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see next page

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 98/00929

There are two inventions claimed in the application:
1. Claims 1-8, 31-33 and 42 relates to a method of manufacturing bipolar transistors having a collector plug, and bipolar transistors according to the method, where said transistors are surrounded by trenches free from dislocation defects.
2. Claims 9-30, 34-41, 43 and 44 relates to a method of manufacturing trenches free from dislocation defects, and trenches manufactured by said method.

The two methods relates to two completely different processes. Thus, the method and the device according to the second invention lack the special technical features to fulfil the requirements for unity of invention with the first invention aprori. See PCT rule 13.2.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte. ational application No.
PCT/SE 98/00929

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0724291 A2	31/07/96	JP 8203994 A	09/08/96
		US 5789769 A	04/08/98
US 4980747 A	25/12/90	EP 0272491 A	29/06/88
		JP 63168032 A	12/07/88
		KR 9700552 B	13/01/97
US 4301588 A	24/11/81	CA 1148273 A	14/06/83
		EP 0033495 A,B	12/08/81
		JP 56114352 A	08/09/81
US 4789885 A	06/12/88	JP 63301562 A	08/12/88
US 5266504 A	30/11/93	NONE	
US 5592412 A	07/01/97	NONE	
WO 9525343 A1	21/09/95	EP 0698284 A	28/02/96
		US 5683932 A	04/11/97
		US 5691232 A	25/11/97
US 5217920 A	08/06/93	NONE	
US 5270265 A	14/12/93	NONE	
US 4958213 A	18/09/90	DE 3855252 D,T	14/08/96
		EP 0320217 A,B	14/06/89
		JP 2002156 A	08/01/90